REMARKS

Claims 1-50, as amended, remain herein. Claims 9-12, 16, 20, 24 and 31 have been amended.

The specification is amended to correct clerical errors which occurred during translation of the Japanese text into the English language.

The claims have been amended to eliminate multiply dependencies.

Examination of this application on its merits is respectfully requested.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

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Date

Roger W. Parkhurst
Registration No. 25,177

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Specification and Claims Mark Ups

RWP/ame

Attorney Docket No. OGOH:076

PARKHURST & WENDEL, L.L.P.
1421 Prince Street, Suite 210
Alexandria, Virginia 22314-2805
Telephone: (703) 739-0220

syndrome calculator 5 outputs the error-containing code detection signal 22, which indicates that an error-containing code word has been detected, to the DMA control unit 2 and to the error detector 7; the error corrector 6 outputs the error-containing code word signal 23 to the DMA control unit 2 and to the error detector 7; and that the mid-term result register 8 is provided.

Figure 9 shows the structure of the error correction device of the present embodiment.

In Figure 9, in response to the output of the error-containing code detection signal 22, the error detector 7 suspends an error detecting process, and the DMA control unit 2 suspends a data transfer from the buffer memory 4 to the syndrome calculator 5. The error corrector 6 outputs an one-code word error correction completion signal 23 when it completes error correction for one code word.

Figure 10 shows the procedure of horizontal error correction in one sector of the error correction device of the present embodiment.

The behavior of the error correction device will be described as follows with reference to Figure 10.

Step (d-1): the same process as at step (c-1) of Embodiment 2 is performed.

Step (d-2): the same process as at step (c-2) of Embodiment 2 is performed.

Step (d-3): the same process as at step ~~(a-3)~~(b-3) of Embodiment 1 is performed.

Step (d-4): the syndrome calculator 5 performs error-containing code

detection for every transferred code word, and outputs the syndrome 16 to the error corrector 6. When an error-containing code word is detected, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error detector 7 and to the DMA control unit 2. On the other hand, the error detector 7 also executes error detection for each code word. Only when the error-containing code detection signal 22 has not been outputted, the mid-term results of error detection for each code word are stored in the mid-term result register 8. When the detection of error-containing code has been informed by the error-containing code detection signal 22, the error detector 7 suspends an error detecting process. At the same time, the syndrome calculator 5 informs the DMA control unit 2 of the detection of an error-containing code. The DMA control unit 2 suspends an output of the DMA request ~~23~~ 13to the bus control unit 3. The bus control unit 3 suspends a data transfer from the buffer memory 4 to the syndrome calculator 5.

Step (d-5): the same process as at step (a-5) in the prior art is performed.

Step (d-6): the same process as at step (b-6) in the first embodiment is performed.

Step (d-7): the same process as at step (a-7) in the prior art is performed.

Step (d-8): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector 6 and overwrites the data in the buffer memory 4. When error correction for one code word is complete, the error corrector 6 transmits the one-code word

transfer range in error detection of the present embodiment.

The behavior of the error correction device 100 of the present embodiment thus structured will be described with reference to Figures 12, 13, and 14.

Step (e-1): in order to perform error correction, the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 so as to provide instructions to transfer data equivalent to one code word in the horizontal direction×13 times, or one sector from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (e-2): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector ~~7~~7.

Step (e-3): the bus control unit 3 puts the data bus 11 in commission, and outputs the buffer memory access signal 14 to the buffer memory 4. The bus control unit 3 then outputs the syndrome data supply signal 15 and the error detector data supply signal 20 to the syndrome calculator 5 and the error detector 7, respectively, so as to supply the data read from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (e-4): the syndrome calculator 5 calculates a syndrome 16 of the transferred horizontal code word, and outputs the syndrome 16 to the error corrector 6. If the code word contains an error-containing code, or if the syndrome is not zero, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error corrector 7 and to the system control unit 1. The syndrome calculator 5 also provides the system

unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. Then, the bus control unit 3 outputs the syndrome data supply signal 15 to the syndrome calculator 5 so as to supply the data read from the buffer memory 4.

Step (f-10): the syndrome calculator 5 calculates the syndrome of each vertical code word in the transferred second ECC block, and outputs the syndrome 16 to the error corrector 6. The syndrome calculator 5 then outputs the error-containing code detection signal 22 to the system control unit 1 when the code word has an error, or when the syndrome 16 is not zero.

Step (f-11): the error corrector 6, after correcting an error in the code, transmits the access request signal 17 to the bus control unit 3 to request writing of the error-corrected data to the buffer memory 4. The error corrector 6 further provides the system control unit 1 with the error correcting position signal 24 indicating the position of the error-corrected data. By using the error correcting position signal 24 and the error-containing code word signal 23 obtained in the first-time error correction, it is determined whether the error correction and the error detection for one ECC block in the third-time error correction should be performed from the beginning or from a halfway point.

Step (f-12): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector ~~61~~6 and writes the data to the buffer memory 4.

The vertical error correction for one ECC block is completed by repeating steps (f-7) through (f-12) as many as the vertical strings shown in

started from the code word on the n-th line indicated by the error-containing code word signal 23 found in the first-time error correction so as to perform syndrome calculation, and in parallel with the syndrome calculation, error detection is performed using the mid-term results of the EDC held in the third mid-term result register 83. On the other hand, when an error in data is corrected within the valid range of the mid-term results of an EDC, the mid-term results of the EDC are invalid, and data transfer is started from the head code word in the sector from which the error-containing code has been detected.

Step (f-13): in order to execute the third-time error correction for the third ECC block, the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 so as to provide instructions to transfer data corresponding to a horizontal code word in the third ECC block from the buffer memory 4 to the syndrome calculator 5 and to the error detector ~~72~~7.

Step (f-14): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector ~~72~~7.

Step (f-15): the bus control unit 3 puts the data bus 11 in commission, and outputs the buffer memory access signal 14 to the buffer memory 4 to read data therefrom. The bus control unit 3 then outputs the syndrome data supply signal 15 and the error detector data supply signal 20 to the syndrome calculator 5 and the error detector ~~72~~7, respectively, so as to supply the data read from the buffer memory 4 to the syndrome calculator 5 and to the error detector ~~72~~7.

Step (f-16): the syndrome calculator 5 calculates a syndrome 16 of the

transferred horizontal code word, and outputs the syndrome 16 to the error corrector ~~616~~ 6. If the code word contains an error-containing code or if the syndrome is not zero, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error detector ~~727~~ 7 and to the system control unit 1. The syndrome calculator 5 also provides the system control unit 1 with the error-containing code word signal 23 indicating the code word from which an error has been detected.

The error detector ~~727~~ 7 executes an error detecting process for the transferred data in parallel with the syndrome calculator 5. Prior to the error detection, the mid-term results of the EDCs in the preceding code words stored in the third mid-term result registers 83 are reloaded. If the syndrome is zero when the transfer of the code words is over, the mid-term results of the EDCs are stored in the third mid-term result register 83 again. When the syndrome is not zero, on the other hand, the mid-term results of the EDCs in the preceding code words are maintained, without updating the contents of the third mid-term result register 83. In the first horizontal code word, the third mid-term result register 83 holds the mid-term results obtained in the first-time error correction. If the detection of an error is informed by the error-containing code detection signal 22, the subsequent code words are not subjected to error detection.

Step (f-17): the error corrector ~~616~~ 6 corrects an error in the code, and transmits the access request signal 17 to the bus control unit 3 to request writing of the error-corrected data to the buffer memory 4.

Step (f-18): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector ~~616~~ 6

and writes them to the buffer memory 4.

Step (f-19): the system control unit 1 outputs the DMA command 12 to the DMA control unit 2 in order to check to see that the error-corrected data contain no error, and provides instructions for data transfer from the buffer memory 4 to the error detector ~~727~~. This data transfer involves data from the code word indicated by the error-containing code word signal 23 outputted together with the error-containing code detection signal 22 outputted first by the syndrome calculator 5 at step (f-4).

Step (f-20): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the error detector ~~727~~.

Step (f-21): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. Then, the bus control unit 3 outputs the error detector data supply signal 20 to the error detector ~~727~~ so as to supply the data read from the buffer memory 4.

Step (f-22): using the mid-term results of the error detection stored in the third mid-term register 83, the error detector ~~727~~ executes error detection of the transferred subsequent data, and transmits the error detection signal 21 to the system control unit 1 so as to inform whether an error has been detected or not.

The error correction for one sector is completed by repeating steps (f-13) through (f-22) 13 times, and the horizontal error correction for one ECC block is completed by repeating this procedure for 16 sectors. In the third-time error correction, if the mid-term results of error detection

correction, and when error correction is difficult, another process would be applied to collective ECC blocks.

(Embodiment 7)

While in Embodiment 6, error correction and error detection are performed in the first-time error correction for a code word temporarily stored in the buffer memory 4, in the present embodiment the first-time error correction and detection are performed in parallel with demodulation. In order to realize this feature, as shown in Figure 18, the error detection device of the present embodiment comprises two syndrome calculators and two error detectors. The error detection device will be described as follows with reference to Figure 18.

The drawing includes the first and second syndrome calculators 51 and 52, and the first and second error detectors 71 and 72. The upstream and downstream units are not illustrated.

The error detection device 100 receives data stored in an optical disk as a reception code 29 from the amplifier. The reception code 29 is entered to the demodulator 10. The demodulated code is stored in the buffer memory 4 by means of the demodulating code input signal 25 outputted from the bus control unit 3, and also supplied to the second syndrome calculator 52 and to the second error detector 72.

In order to perform error correction and error detection with the code word read from the buffer memory 4, the first syndrome calculator 51 and the first error detector 71 are arranged separately. The input of the error corrector ~~616~~ 616 is connected to a selection circuit 60 so that the error corrector ~~616~~ 616 can select between the syndromes transmitted from the first

and second syndrome calculators 51 and 52.

The second syndrome calculator 52 calculates a syndrome 162 of each transferred horizontal code word, and outputs the syndrome 162 to the error corrector ~~61~~6. If the code word contains an error-containing code or if the syndrome 162 is not zero, the second syndrome calculator 52 outputs the error-containing code detection signal 222 to the second error corrector 72 and to the system control unit 1. The second syndrome calculator 52 also provides the system control unit 1 with an error-containing code word signal 232 indicating the code word from which an error has been detected.

The second error detector 72 executes an error detecting calculation for the transferred data in parallel with this.

When the second syndrome calculator 52 detects an error-containing code word, the error corrector 6 performs error correction, and the results are written in the buffer memory 4. Then, vertical error detection and correction and the second-time and later horizontal error detection and correction are executed by the first syndrome calculator 51 and the first error detector 71. Prior to the error detection, the mid-term results of the EDCs in the preceding code words stored in the mid-term result register assigned in the pipeline processing are reloaded. If the syndrome is zero when the transfer of the code words is over, the mid-term results of the EDCs are stored in the mid-term result register again. When the syndrome is not zero, on the other hand, the mid-term results of the EDCs in the preceding code words are maintained, without updating the contents of the mid-term result register.

Figure 19 conceptually shows changes in the contents (structure, flow)

means detects an error-containing code; and for making one of said syndrome calculating means and said error correcting means provide said system control means with information which designates the code word including the error-containing code; and

a number-of-times control sub means for repeating the odd-numbered error correction and the even-numbered error correction a predetermined number of times.

8. The error correction device of claim 7, wherein said number-of-times control sub means is a three-time repetition control sub means for repeating the error correction three times at most.

9. The error correction device of claim 7 ~~or 8~~ further comprising a storing means for storing mid-term results, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a non-error sector code word range designating sub means for designating, in code word units of a sector, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and on said information that designates the position of the error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of the sector from which an error-containing code has been detected, based on the information designated by said non-error sector code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said storing means as an initial value.

10. The error correction device of claim 7 ~~or 8~~ further comprising a sector-basis storing means for storing mid-term results, on a sector-by-sector basis, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means, until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a sector-basis non-error code word range designating sub means for designating, on a sector-by-sector basis, in code word units, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and on said information that designates the position of the error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of each sector from which an error-containing code has been detected, based on the information designated by said sector-basis non-error code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said sector-basis storing means as an initial value.

11. The error correction device of claim 7 ~~or 8~~ further comprising a sector-group-basis storing means for storing mid-term results, on a sector-group-by-sector-group-basis, in code word units, of each code word from which no error has been detected in the error detecting process done by said error detecting means until said syndrome calculating means detects an error-containing code, wherein

said non-error range designating sub means is a sector-group-basis non-error code word range designating sub means for designating, on a sector-group-by-sector-group-basis, in code word units, a range from which an error-containing code has not been detected in the odd-numbered error correction or the subsequent even-numbered error correction, based on said information that designates the code word including the error-containing code and on said information that designates the position of the

error-containing code in the error correcting code word; and

said odd-numbered error correction sub means is an odd-numbered error correction sub means with mid-term results for, in the third-time or later odd-numbered error correction, making said bus control means start a concurrent data transfer not at the head but at the code word of each sector group from which an error-containing code has been detected, based on the information designated by said sector-group-basis non-error code word range designating sub means; for making said syndrome calculating means start syndrome calculation at the code word; and for making said error detecting means start error detection at a code word somewhere in the middle of the sector by using contents stored in said sector-group-basis storing means as an initial value.

12. The error correction device of claim 1, ~~2, 5, 6, 7, or 8,~~ wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting

means that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

16. The error correction device of claim 1, ~~2, 5, 6, 7, or 8,~~ wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

an means-basis ECC block pipeline processing notification sub means for transmitting ECC blocks which have been subjected to error correction

downstream; for storing ECC blocks to be processed next to said ECC-block-basis buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means in said system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the code words which are to be processed therein.

an ECC block code word recognition sub means in sub means-basis pipeline processing for making said first error detecting sub means, said even-numbered error correction sub means, said even-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means in said system control means recognize that the error-corrected ECC blocks have been transmitted downstream and new ECC blocks to be processed have been stored in said ECC-block-basis buffer memory, and further making these same sub means contained in said system control means recognize the ECC blocks and the code words which are to be processed therein.

20. The error correction device of claim 1, ~~2, 5, 6, 7, or 8~~ wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block

basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block recognition sub means for recognizing a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; for recognizing the error correction done by said error correcting means; for recognizing writing of error-corrected data to said plural-ECC-block-division buffer memory by said bus control means; for recognizing ECC blocks in process when said error detecting means stores mid-term results to said plural-ECC-block-division storing means, and for selecting ECC blocks to be processed; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively

transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

21. The error correction device of claim 9 wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction, wherein

said buffer memory is a plural-ECC-block-division buffer memory corresponding to a plurality of ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-division storing means for storing said plurality of ECC blocks on a block-by-block basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer

be processed; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

24. The error correction device of claim 1, ~~2, 5, 6, 7, or 8,~~ wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code

word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

a collective-type means-basis ECC block pipeline processing notification sub means for collectively transmitting ECC blocks which have been subjected to error correction downstream; for collectively storing ECC blocks to be processed next to said plural-ECC-block-division buffer memory; and for making the storage known to said bus control means, said syndrome calculating means, said error detecting means, and said error correcting means;

a collective-type means-basis ECC block code word recognition sub means for selecting code words of the ECC blocks to be processed, in accordance with the contents stored in said ECC-block-and-code word-division storing means, in controlling a data transfer from said bus control means to said syndrome calculating means, to said error detecting means, and to said error correcting means for error detection and error correction; in controlling the error correction done by said error correcting means; in controlling writing of error-corrected data to said ECC-block-basis buffer memory done by said bus control means; in storing mid-term results to said ECC-block-and-code word-division storing means by said error detecting means; and

a collective-type ECC block notification sub means in sub means-basis pipeline processing for notifying said first error detecting sub means, said even-numbered error correction sub means, said odd-numbered error

correction sub means, said number-of-times control sub means, and said DMA transfer instruction sub means contained in said system control means that the error-corrected ECC blocks have been collectively transmitted downstream and new ECC blocks to be processed have been collectively stored in said plural-ECC-block-division buffer memory, and further notifying these same sub means contained in said system control means of the ECC blocks which are in process therein.

25. The error correction device of claim 9, wherein error correction is performed in parallel for data in a plurality of ECC blocks each having a structure where a plurality of error correcting code words each comprising a data unit and a parity unit are arranged in vertical direction and horizontal direction so as to repeat error correction a plurality of number of times, and where predetermined data composed of a predetermined number of code words in the vertical direction or the horizontal direction (data in the horizontal direction are referred to as sector) as a unit are subjected to the error correction;

said buffer memory is an ECC-block-basis buffer memory for storing, on a block-by-block basis, ECC blocks to be processed in parallel;

said storing means for storing mid-term results of an error detecting process generated by said error detecting means is an ECC-block-and-code word-division storing means for storing ECC blocks in process on a block-by-block basis, and code words in each ECC block, in each sector, or in each sector group, on a string-by-string basis;

said system control means comprises:

to be processed in said buffer memory.

31. The error correction device of claim 1, ~~2, 3, 4, 5, 6, 7, 8, 28, 29, or 30~~ further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

32. The error correction device of claim 9 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.